High-volume full-wafer step-and-flash imprint lithography

S-FIL is a unique method for printing sub-100nm geometries [1-3]. When high-resolution alignment is needed, the S-FIL process uses field-to-field drop dispensing of UV curable liquids for step-and-repeat patterning. A full substrate patterning process can better serve applications such as patterned media, photonic crystals, and wire grid polarizers since the alignment requirements are minimal. In general, the substrates employed in these markets do not have the stringent flatness specifications needed for silicon integrated circuit (IC) fabrication. As a result, the imprinting of nanoscale features becomes particularly challenging, especially when imprinting with thick templates.

Patterning challenges

The lithographic requirements to image both photonic crystal and patterned media devices are extremely challenging. Each application presents unique problems for a more conventional optical projection approach. Photonic crystals, with periods comparable to the optical wavelength within a light emitting diode (LED), employ diffractive effects to couple out light that is otherwise unavailable, enhancing the overall efficiency of the LED. Photonic crystals can improve the efficiency of LEDs through two different mechanisms: improvement of the radiative efficiency of the device and improvement of the extraction efficiency [4]. Photonic crystal lattices typically require pitches considerably <1:1. In addition, the patterns are most effective when done by applying more randomized super dense arrays with a minimum feature size approaching sub-50nm (**Fig. 1**), as opposed to the repeating cell structures printed by reduction scanners for CMOS devices.

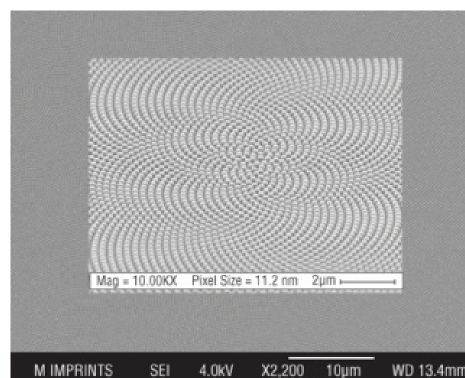

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Figure 1. *Photonic crystal array. The inset shows a close-up of the imprinted features. Crystal designed by Mesophotonics.*

Patterned media are particularly challenging because of the aggressive feature sizes necessary to achieve storage densities required for manufacturing beyond the current technology of perpendicular recording. The first insertion opportunity for patterned media is expected to be at features with a half-pitch of = 18nm, with an anticipated entry point around 2010. In comparison, the *International Technology Roadmap for Semiconductors* (*ITRS*) for DRAM storage presently calls for a 17nm half-pitch (hp) for production in 2018.

Fabrication challenges

It is important to note that the production methods currently used to fabricate silicon ICs will not be capable of resolving sub-17nm geometries. Extensions to 193nm immersion lithography, such as extreme ultraviolet (EUV) lithography, may be capable of achieving this resolution, but will not be ready by 2010 and will come with a price tag ($50-$65M) that is prohibitive. Multiple-beam direct-write electron beam lithography is another alternative approach. Even if these systems can be perfected in the next few years, it is extremely unlikely they will ever be able to provide the throughput required for the media industry. Ultraviolet imprint lithography, and specifically S-FIL, is the only nanopatterning method that: 1) has the inherent resolution necessary to define sub-10nm geometries [5], 2) can be ready for production in the required timeframe, and 3) has a cost structure commensurate with patterned media.

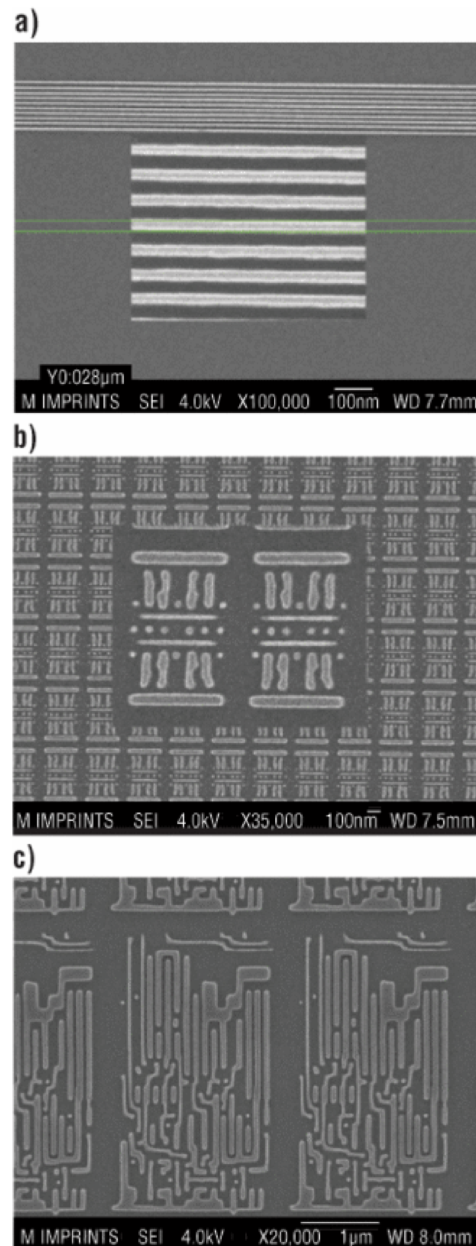

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***Figure 2.**. Imprinted features using step-and-flash imprint lithography for a) 32nm lines, **b)** 32nm Metal 1 lines, and **c)** 32nm logic structures.*

Previous work has demonstrated that a conventional template fabrication flow can yield CMOS features with half-pitches = 32nm [6]. Examples are shown in **Fig. 2**. In this paper, we describe creating a thin template suitable for either full wafer or disk imprinting. Dense arrays of holes with half-pitches as small as 21nm were imaged using an S-FIL approach. Techniques for further enhancing the pattern density as well as a method for addressing feature image placement are described. Finally, a process for replicating a master template is discussed in detail.

Experimental details

A lift-off process was employed to achieve resolutions better than 28nm. All patterning was done on 150mm dia. fused silica wafers. Charging during electron beam exposure can be addressed by either applying a conductive topcoat on the e-beam resist, or by depositing a conducting layer beneath the resist. In this study, the latter method was employed. To generate the template relief images, patterns were exposed using a Vistec VB6 100keV Gaussian beam writer. Poly(methyl methacrylate) (PMMA) resist was chosen as the positive imaging resist. After development, a thin chromium layer was evaporated, followed by a lift-off using dichloromethane. The remaining chromium features served as a hard mask for etching into the fused silica.

Imprinting of the template pattern was performed using a Molecular Imprints Imprio-1100 full wafer imprinting system. The tool supports the imprint process on 2-4 in. substrates and is capable of running in a fully automated mode at manufacturing throughputs in excess of 20wph. With the appropriate engineering modifications, scaling to larger substrates size is also possible.

A drop-on-demand method was employed to dispense the photo-polymerizable acrylate based imprint solution. The template was then lowered into liquid contact with the substrate, displacing the solution and filling the imprint field. UV irradiation through the backside of the template cured the acrylate monomer. Details of the imprint process have previously been reported [7].

Results and discussion

Master template fabrication. Starting with a conductively coated fused silica substrate, the template fabrication process can be broken into five key steps:

1. Resist exposure and develop
2. Resist descum
3. Chromium deposition
4. Lift-off
5. Pattern transfer into the fused silica

The primary patterns of interest were dense arrays of holes, starting at a maximum feature size of 27nm hp. The PMMA resist was exposed by negatively biasing the critical features and increasing the exposure dose. Previous work done in ZEP520A resist has demonstrated that this is a very effective method for increasing process latitude during the exposure process [8].

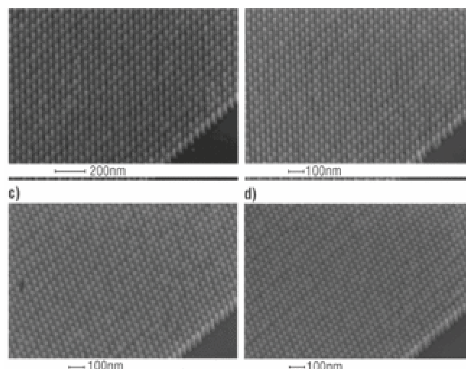

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Figure 3. *Template features after the fused silica etch at* ***a)*** *27nm, b) 25nm,* ***c)*** *23nm, and* ***d)*** *21nm. Dense features*

with a half-pitch as small as 21nm were clearly resolved.

The template features are defined using a reactive ion etch process. The etchant gases include CHF_3 and oxygen. The resulting features are shown in **Fig. 3**. The features are well defined, with a minimum of defective areas. Occasional image placement problems were noted, however. In addition, there were several instances where the chromium did not adhere well to the substrate, resulting in a missing pillar after the fused silica etch; one example of this can be observed in Fig. 3c. The image profile is also less than optimal. It is likely that some erosion of the chromium mask occurs during the fused silica etch. A wall angle of better than 87° is preferred, and optimization of the etch process will be a subject for future investigation.

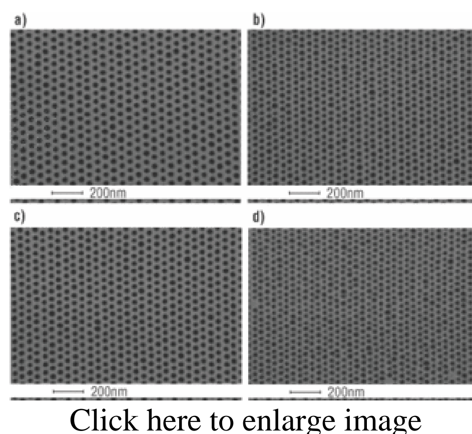

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Figure 4. *Imprinted patterns at* ***a)*** *27nm hp,* ***b)*** *25nm hp,* ***c)*** *23nm hp, and* ***d)*** *21nm hp.*

Imprint results. After pattern transfer of the pillars was complete, the resulting templates were used for imprint studies. The results are depicted in **Fig. 4.** Good uniformity was noted for the 27nm and 25nm arrays. More irregularities occur in the smaller features, and include CD nonuniformity, image placement errors, and missing holes. In general, the imprint process faithfully replicated the features on the template.

Pattern density enhancements. It is likely that minor improvements can be made in the PMMA process to further increase pattern density. The resist can be thinned further to minimize forward scattering during electron beam exposure. Techniques such as cold development can also improve resist contrast [9]. Alternative resists may be necessary to approach a 10nm hp, however.

Hydrogen silsesquioxane, or HSQ, has been used by several researchers to minimize feature critical dimensions [10]. HSQ is a negatively acting glass-like resist. The U. of Cambridge has recently demonstrated 12.5nm hp arrays on silicon substrates. As a result, a straightforward subtractive pattern transfer process c an be employed after resist imaging.

It is possible that an approach other than electron beam lithography will be required for half-pitches <10nm. One possible method for achieving this resolution is scanning probe lithography, in which a sharply defined tip is used to mechanically deform a resist such as PMMA. Resolution of <3nm has been demonstrated at MIT [11]. To employ this technique for master template patterning will likely require a multitip approach in order to obtain any sort of reasonable writing times.

As pattern densities shrink well below a half-pitch of 18nm, the pattern placement required of either electron beam or scanning probe systems will need to drastically improve. Moon et al. have tested a method called interferometric spatial phase imaging (ISPI) to achieve this sort of image placement [12]. In ISPI, position information is encoded in the spatial phase of interference fringes. An interferometric moiré pattern is formed by the interference of beams diffracted from periodic structures on the mask and substrate. Further work will be required to optimize the application and integrate the method, but the approach does offer a solution to a very difficult problem.

Template replication. Creating a master template is only the first step towards solving the template supply issue for either patterned media or LEDs. It is likely that several hundreds imprint tools will be needed to produce the required number of patterned GaN coated wafers (in the case of LEDs) and disks (for patterned media). Each imprint tool, in turn, will need multiple copies of a template to insure defect-free imprinting over the course of a particular design rule. As a result, it is conceivable that well over 1000 templates will be required for any one generation of patterned media. Given that writing time for a master may take as long as 24-48 hours, the industry is faced with two problems. The first is writing all the required templates in a reasonable timeframe. The second is the exorbitant cost for every e-beam written template.

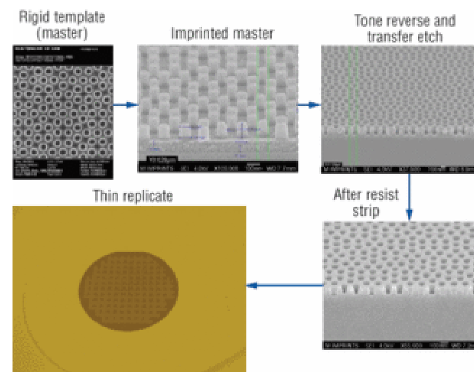

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Figure 5. *Process flow for template replication. In this case, a rigid template was used to create a thin conformal template.*

A better approach is to create a master template, and use the imprint tool to form replicate templates. This technique has recently been demonstrated for photonic crystal arrays [13]. The method is reviewed below.

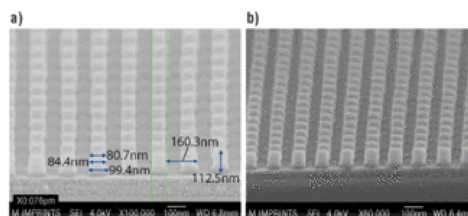

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Figure 6. *Imprint from **a)** the master template, and **b)** the replicate template.*

The tone of the master template is maintained by employing an S-FIL/R (reverse tone) pattern transfer process [14, 15]. The process steps are depicted in **Fig. 5**. To create the replicate template, the patterns are imprinted onto an organic transfer layer and chromium coated 6 in. fused silica wafer. A high silicon content resist, SilSpin, is spun on to planarize the organic monomer material. Following an etch back of the SilSpin, the monomer and transfer layer are patterned using the SilSpin as a hard mask. The Silspin and monomer stack then serves as a masking layer for the chrome and fused silica etches. The remaining monomer and chrome are then removed to create a thin conformal replicate template.

A finished replicate template was imprinted on an Imprio-1100 full wafer imprint system that is currently configured to print 2-4 in. wafers. An example of an imprint from the replicate template is shown in **Fig. 6b**. For comparison, the original imprint from the master template is shown in **Fig. 6a**. Note that the critical features and pitch are comparable for both imprints. Wall angle from the replicated pattern is also comparable to the original, with the additional advantage that there is no evidence of microtrenching in the fused silica etch.

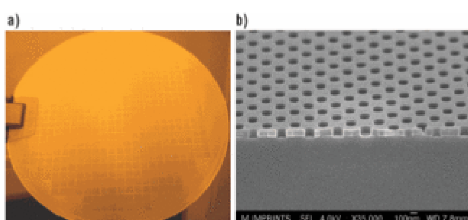

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Figure 7. *A 3 in. sapphire wafer* ***a)*** *imprinted and* ***b)*** *patterned after the hardmask etch; the resist is still intact.*

The resulting imprinted sapphire wafer with the complete patterned array of photonic crystals is shown in **Fig. 7a** (also see **Fig. 1**). Note the uniform color in the imprinted resist, indicating minimal variation in the imprinted residual layer. The process is considered complete after tone reversal, a dry etch of the monomer and transfer layer and an etch into a hardmask and the underlaying GaN. Figure **7b** depicts a processed LED wafer after the hardmask etch.

Conclusion

A technique for creating high density master templates for patterned media was presented. Half-pitches of 21nm using a PMMA lift-off process were formed on a template and imaged using an Imprio-1100 step-and-flash imprint lithography full wafer production tool. Techniques for achieving even greater pattern densities will be necessary for a viable patterned media product, and two different options for achieving these densities were discussed. Also required is an improvement in feature image placement on the master template. ISPI is a potential solution which still requires integration into a commercial writing tool. Finally, a method for fabricating replicate templates was presented. One topic not discussed was the inspection techniques needed to qualify a master template. Electron beams can also be used for inspection, and work will be required to verify that an electron beam inspection system can be applied at dimensions = 18nm.

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References

1. M. Colburn, S. Johnson, M. Stewart, S. Damle, T. Bailey, B. Choi, et al., *Proc. SPIE, Emerging Lithographic Technologies III,* 379, 1999.
2. T.C. Bailey, D.J. Resnick, D. Mancini, K.J. Nordquist, W.J. Dauksher, E. Ainley, et al., *Microelectronic Engineering,* Vol. 61-62, pp. 461-467, 2002.
3. W.J. Dauksher, K.J. Nordquist, D. Mancini, D.J. Resnick, J.H. Baker, A.E. Hooper, et al., *J. Vac. Sci. Technol.* B 20(6), pp. 2857-2861, 2002
4. J.J. Wierer, M.R. Krames, J.E. Epler, N.F. Gardner, J.R. Wendt, M.M. Sigalas, et al., *Proc. SPIE,* Vol. 5739, pp. 102-107, 2005.
5. F. Hua, Y. Sun, A. Gaur, M.A. Meitl, L. Bilhaut, L. Rotkina, et al., *Nano Lett.,* 4(12), pp. 2467-2471, 2004.
6. G.M. Schmid, D.J. Resnick, E.D. Thompson, L.J. Myron, D.L. Olynick, J.A. Liddle, et al., *International Symposium on Electron, Ion, and Photon Beam Technology, and Nanobfabrication*, June 2006.
7. M. Colburn, T. Bailey, B.J. Choi, J.G. Ekerdt, S.V. Sreenivasan,C.G. Willson, "Development and Advantages of Step-and-flash Lithography," *Solid State Technology,* 67, July 2001.
8. G.M. Schmid, E. Thompson, N. Stacey, D.J. Resnick, D.L. Olynick, E.H. Anderson, to be published in *Microelectronic Engineering*, 2007.
9. W. Hu, K. Sarveswaran, M. Lieberman, G.H. Bernstein, *J. Vac. Sci. Technol.* B 22, 4, July/Aug. 2004.
10. H. Namatsu, T. Yamaguchi, M. Nagase, K. Yamazaki, K. Kurihara, *Microelectronic Engineering,* 41/42, pp. 331-334, 1998.
11. E.E. Moon, P.N. Everett, H.I. Smith, to be published in *J. Vac. Sci. Technol.* B, Nov./Dec., 2006.
12. E.E. Moon, M.K. Mondol, P.N. Everett, H.I. Smith, *J. Vac. Sci. Technol.* B, 23, 749, 2005.
13. M. Miller, G. Schmid, G. Doyle, E. Thompson, D.J. Resnick, to be published in *Microelectronic Engineering,* 2007.
14. M. Miller, G. Doyle, N. Stacey, F. Xu, S.V. Sreenivasan, M. Watts, et al., *Proc. SPIE* 5751, 994, 2005.
15. S.V. Sreenivasan, I. McMackin, F. Xu, D. Wang, N. Stacey, D. Resnick, "Using Reverse-tone Bilayer Etch in Ultraviolet Nanoimprint Lithography," *Micro Magazine*, Jan./Feb. 2005.

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